UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/855,641	05/15/2001	Jeremy E. San	1248-29	1734

27562 7590 06/13/2006

NIXON & VANDERHYE, P.C.
901 NORTH GLEBE ROAD, 11TH FLOOR
ARLINGTON, VA 22203

EXAMINER	
WU, XIAO MIN	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 06/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/855,641	SAN ET AL.	
	Examiner	Art Unit	
	XIAO M. WU	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *80-82 and 84-223* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *80-82 and 84-223* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 80-82 and 84-203are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-11 of U.S. Patent No. 6,646,653. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following reasons.

Claim 80 is a representative claim of the instant application and claim 1 and 4 are representative claims of US Patent No. 6,646,653. the comparison is illustrated as follow:

Claim 1of US 6,646,653	Claim 80 of instant application
1. An information processing system including a display and a first processing unit for executing at least a first portion of a video graphics	80. A home video game system for use with a television type monitor display device, said system contained, at least in part, in a housing having an

program, said video graphics program being received from an external source, and including a second portion having instructions relating to 3-D graphics operations, and a programmable graphics processor separate from said first processing unit comprising: means for receiving instructions from said second portion of said video graphics program; and means for executing said instructions from said second portion of said video graphics program, whereby said graphics processor coacts with said first processing unit to control 3-D display of an object. 4. An information processing system according to claim 1, wherein said external source comprises an external memory.	instruction port for receiving a removable storage device, comprising: a programmable graphics processor; a main processor that executes at least a portion of video graphics generating game program that includes instructions for displaying polygon-based 3D graphics objects and which communicates information relating to one or more polygon-based 3D graphics objects to said programmable graphics processor, wherein the programmable graphics processor is contained within the removable memory storage device and is programmed to render at least one or more portions of said 3D polygon-based graphics objects for display on said display device.

Form the comparison above, it is noted that Claims 1 and 4 from patent # 6,646,653 include a display, first processing unit for executing at least a first portion of video graphics program and a programmable graphics processor that co-acts with first processing unit to control 3-D display of an object. Claim 80 of the present application includes a programmable graphics processor and a main processor that communicates with the programmable graphics processor. Therefore conflicting claims are not patentably distinct from each other.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 80, 135, 206 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent 5,016,876 to Loffredo in view of US Patent 5,190,285 to Levy et al., hereafter "Levy".

Regarding independent claim 80, "A home video game system for use with a television type monitor display device, said system contained, at least in part, in a housing having an insertion port for receiving a removable memory storage device, comprising:

a programmable graphics processor; (Loffredo disclose in col. 4 lines 50-60 and in Fig. 1 as "a digital computer 22")

a main processor that executes at least a portion of a video graphics generating game program that includes instructions for displaying polygon-based graphics objects and which communicates information relating to one or more polygon-based 3D graphic objects to said programmable graphics processor, (Loffredo disclose in Fig. 1 as "DMA coprocessor 130")

wherein the programmable graphic processor is contained within the removable memory storage device and is programmed to render at least one or more portions of said 3D polygon-based graphic objects for display on said display device (Loffredo disclose in col. 9 lines 23-38 and also in col. 1 lines 50-60).
Loffredo does not explicitly disclose removable memory storage device. Levy discloses in col. 6 lines 21-23 a game system that includes a game processor 80, in col. 7 lines 11-14 graphics processor 94 and in col. 6 lines 42-47 an external unit 92. It would have been obvious to one of ordinary skill in the art at the time of invention to substitute the memory storage of Loffredo with the removable memory as taught by Levy to improve the video game by permitting existing processors to address a larger program memory address space.

Independent claim 135 is rejected under the same rationale as independent claim 80 above; further the limitation "Video RAM" is disclosed by Loffredo in col. 6 lines 13-21.

Independent claim 206 is the same as claim 80, therefore is rejected under the same rationale.

6. Claims 81-134, 136-205, 207-223 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent 5,016,876 to Loffredo in view of US Patent 5,190,285 to Levy et al., hereafter "Levy" and further in view of "PC TECH JOURNAL, "Custom-Tailored Graphics: TMS 34010, by Ed McNierney, July 1987, Pages 68-74; hereafter McNierney.

Regarding claims 81, 99, 118, 136, 155, 173, 188 and 207 the combination of Loffredo with Levy teaches the claimed invention. Furthermore Loffredo discloses in col. 4 lines 49-62 "Texas Instruments Graphics System Processor TMS34010 ("GPS")" but does not disclose the internal architecture of the GPS and therefore the TMS34010's ability to respond to specific instructions used for rendering 3D objects are not clearly disclosed. However, McNierney discloses in page

68-74 TMS34010 "GPS" internal architecture that includes a coprocessor that has a highly pipelined internal architecture, a high-speed arithmetic logic unit and programmable 256-byte instruction cache and a 32 bit barrel shifter that allows it to fetch instructions in parallel with executing instructions and accessing registers and local memory. responsive to specific instructions used for rendering 3D objects.

It would have been obvious to one of ordinary skill in the art at the time of invention to refer, use and rely on McNierney's discloser to illustrate TMS34010 GPS's ability to respond to specific instructions (transformation, clipping and lighting of the initial object) used for rendering 3D objects and thus illustrating Loffredo's system ability to be responsive to 3D rendering instructions.

Regarding claims 82-96,100-115, 119-133, 137, 149, 156-170, 174-184, 189- 201, 208-222; the combination of Loffredo with Levy teaches the claimed invention. Further McNierney discloses in page 68 last column last paragraph TMS34010 that is a pipelined processor and includes an Arithmetic Logic Unit, barrel shifter (multiplier unit that performs multiply operation using at least 16-bit length, a cache RAM and plurality of registers and also is capable of performing graphics-intensive tasks like rotation or scaling of polygon based objects. In addition the GPS TMS34010 include the pixel plotting circuit (McNierney page 68-70), and it includes a set of instructions (McNierney page 71) an instruction for texture mapping and an instruction for controlling transparency of display object and an instruction for fractional signed multiply instruction are included in the set (McNierney page 73).

McNierney also discloses in page 71 Fig. 2 that graphics processor incorporates an Arithmetic Logic Unit, cache Ram, high speed multiplier and plurality of registers fabricated on a single chip.

Regarding claims 97, 116, 134, 153, 171, 185 and 223, "...further comprising a CD ROM reader device..." Loffredo does not explicitly disclose a CD ROM reader device. Levy discloses a game system that includes a game processor 80, graphics processor 94 and external unit 92 (Levy discloses in col. 10 lines 58-66 "a program memory detachably connected to the main processor for storing program data associated with an activity to be simulated by the main processor, ..., and program instructions for execution by the main processor for causing the main processor to simulate an activity"); a program memory detachably connected to the main processor may be a CD ROM storage systems that are well known to those skilled in the art.

It would have been obvious to one of ordinary skill in the art at the time of invention to substitute the memory storage of Loffredo with the removable memory as taught by Levy to improve the video game by permitting a different game memory with instructions and data for a different game to be substituted.

Regarding independent claim 98, the combination of Loffredo with Levy teaches the claimed invention as discussed in independent claim 80's rejection above. Furthermore, Loffredo discloses in col. 5 line 54- col. 6 line 67 and in col. 9 lines 23-31 pixel processing by the programmed graphics processor (Also this limitation is disclosed by McNierney in page 68 last column lines 5-8).

Regarding independent claim 117, the combination of Loffredo with Levy teaches the claimed invention as discussed in independent claim 80's rejection above. Furthermore McNierney discloses in page 71 Fig. 2 and 3 a programmable processor having embedded RAM cache memory.

Regarding claims 138, 203 and 205, Loffredo discloses in col. 3 lines 24-27 DMA transfer of pixel data to video RAM.

Regarding independent claim 154, the combination of Loffredo with Levy teaches the claimed invention as discussed in independent claim 80's rejection above. Furthermore, McNierney discloses in page 68 last column, last paragraph a graphics processor including an Arithmetic Logic Unit and geometry transformation circuitry.

Regarding independent claim 172, the combination of Loffredo with Levy teaches the claimed invention as discussed in independent claim 80's rejection above. Furthermore, McNierney discloses in page 68 last column-page 70 first column a programmable pipelined processor having an Arithmetic Logic Unit, barrel shifter (multiplier unit), a cache RAM and plurality of registers and further discloses that the TMS34010 performs graphics-intensive tasks and since image rotation or scaling on polygon based objects is one of graphics-intensive tasks therefore TMS34010 performs them as well.

Regarding independent claims 186, 202 and 205, the combination of Loffredo with Levy teaches the claimed invention as discussed in independent claims 135 and 172's rejection above. Furthermore, McNierney discloses in page 70 the first and second column computing display screen position coordinates for the rotated/or scaled polygon-based object; further Loffredo

teaches in col. 5 line 54- col. 6 line 25 writing pixel color information corresponding to the rotated/ or scaled polygon-based object to the video RAM and further

Response to Arguments

7. Applicant's arguments filed 4/2/2006 have been fully considered but they are not persuasive.

With respect to the obviousness double patenting rejection, applicant argues that claim 80 require "housing having an insertion port for a removable memory" and these features are not recited in claims 1, 2 and 4 of US 6,646,653. This argument is not persuasive because claim 4 requires an external memory. It would have been obvious to have an insertion portion in the computer for receiving the external memory since the computer is communicated with the external memory.

With respect to the 103 rejection, applicant argues that the Loffredo does not show or suggest the rendering of polygon-based 3D graphics objects for display, as set forth in applicant's claims. This argument is not persuasive because Loffredo clearly discloses that the processor22 is preferably a Texas Instruments Graphics System Processor TMS34010. However, it is well known in the art that the TMS34010 processor can process control the polygon-3D graphics object displaying on the screen. Applicant further argues that Loffredo's DMA coprocessor will not function as "main processor". This argument is not persuasive because Loffredo discloses that the DMA is a coprocessor to other processor such as digital computer 20. Thus, either DMA or digital computer can be called as a main processor. Furthermore, applicant argues that McNierney does not discuss the 3D graphics related instruction (e.g. shading, rotating, scaling). This argument is not persuasive. It is well known in the art the Graphics System Processor (TMS34010) can generate polygon-based 3D graphics

object involving shading, rotation and scaling such support can be found in the US Patent No. 5,415,549 to Logg.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The US Patent No. 5,415,549 is cited to support the teaching of the processor TMS34010 including polygon-based 3D graphics objects involving shading, rotation and scaling.

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to XIAO M. WU whose telephone number is 571-272-7761. The examiner can normally be reached on 6:30 am to 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, RICHARD HJERPE, can be reached on 571-272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

x.w.
June 10, 2006

XIAO M. WU
Primary Examiner
Art Unit 2629